REMARKS

The following remarks are made in response to the Office Action mailed Mar. 23, 2006. Claims 1-32 were rejected. With this Response, claims 1, 4, 8, 10, 15-17, 18, 23, 25, and 28 have been amended. Claims 13, 14, 19, 21, 22, and 24 have been canceled without prejudice as to the subject matter contained therein. Claims 1-12, 15-18, 20, 23, and 25-32 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

Claims 1-5, 7, 10-14, 16, 18-32 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,983,361 (Blandy).

Claim 1 as amended recites, *inter alia*:

> a feature indicator associated with at least one of a first sequence of one or more instructions;
> a first register;
> a second register; and
> an execution core;
> wherein the feature indicator indicates whether the execution core supports the at least one of the first sequence of one or more instructions, wherein the execution core is configured to execute a first instruction to cause the first register to be set to a first value using the feature indicator and to cause the second register to be set to a second value using the feature indicator, wherein the execution core is configured to execute the first sequence of one or more instructions to cause a function to be performed in response to the first value in the first register indicating a true condition, and wherein the execution core is configured to execute a second sequence of one or more instructions to cause the function to be performed in response to the second value in the second register indicating the true condition.

Blandy does not teach or suggest "wherein the feature indicator indicates whether the execution core supports the at least one of the first sequence of one or more instructions" as recited in claim 1. In addition, Blandy does not teach or suggest "wherein the execution core is configured to execute a first instruction to cause the first register to be set to a first value

using the feature indicator and to cause the second register to be set to a second value using the feature indicator" as recited in claim 1.

Blandy teaches "an apparatus and method for implementing switch instructions in an IA64 architecture", col. 4, lines 43-45, and "a mechanism by which switch instructions may be implemented in the IA64 architecture", col. 5, lines 32-34. Blandy also teaches that "[t]he present invention will be described with reference to the JAVA bytecode tableswitch." Col. 5, lines 34-35. Although the Office Action makes reference to "mask data used as part of an instruction" with reference to both the "feature specifier" of claim 4 and the "features indicator" of claim 7 (Office Action pp. 3-4; Blandy, col. 6, lines 22-37), the mask of Blandy does not "indicate[] whether the execution core supports the at least one of the first sequence of one or more instructions" as recited in claim 1. Accordingly, Blandy does not teach or suggest "wherein the feature indicator indicates whether the execution core supports the at least one of the first sequence of one or more instructions" as recited in claim 1.

Because Blandy does not teach or suggest "the features indicator" recited in claim 1, Blandy also does not teach or suggest "wherein the execution core is configured to execute a first instruction to cause the first register to be set to a first value using the feature indicator and to cause the second register to be set to a second value using the feature indicator" as recited in claim 1.

Accordingly, Applicants respectfully submits that claim 1 patentably distinguishes over the cited references for at least these reasons. Claims 2-5 and 7 depend from claim 1 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1-5 and 7 under 35 U.S.C. §102(e).

Claim 10, as amended, recites "a processor that includes ... a feature indicator that indicates whether the processor supports at least one of a first sequence of one or more instructions" and "a memory that includes a code segment ... wherein the code segment comprises ... a first instruction configured to cause the first and second predicate registers to be set to first and second values, respectively, according to a third value of the feature indicator".

Applicants respectfully submit that claim 10 patentably distinguishes over the cited references for at least the reasons given above for claim 1. Claims 11, 12, and 16 depend from claim 10 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 10-12 and 16 under 35 U.S.C. §102(e).

Claim 18, as amended, recites "setting a first predicate register of the processor to a first value according to a bit in a features register that indicates whether the processor supports at least one of a first sequence of one or more instructions in response to executing a first instruction that includes a feature specifier that identifies the bit" and "setting a second predicate register of the processor to a second value according to the bit in response to executing the first instruction".

Applicants respectfully submit that claim 18 patentably distinguishes over the cited references for at least the reasons given above for claim 1. Claim 20 depends from claim 18 and is believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 18 and 20 under 35 U.S.C. §102(e).

Claim 23, as amended, recites "a program executable by a processor to cause the processor to: insert a first instruction into a code segment, the first instruction configured to cause first and second predicate registers to be set to first and second values, respectively, according to a feature indicator in the processor that indicates whether the processor supports at least one of a first sequence of one or more instructions".

Applicants respectfully submit that claim 23 patentably distinguishes over the cited references for at least the reasons given above for claim 1. Claims 25-27 depend from claim 23 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 23 and 25-27 under 35 U.S.C. §102(e).

Claim 28, as amended, recites "a feature indicator that indicates whether the processor supports at least one of a first sequence of one or more instructions".

Applicants respectfully submit that claim 28 patentably distinguishes over the cited references for at least the reasons given above for claim 1. Claims 29-32 depend from claim

28 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 28-32 under 35 U.S.C. §102(e).

Claim Rejections under 35 U.S.C. § 103

Claims 6, 15, and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Blandy in view of U.S. Patent No. 6,009,512 (Christie).

Claims 8 and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Blandy in view of U.S. Patent No. 6,918,030 (Johnson).

Applicants respectfully submit that neither Christie nor Johnson teach or suggest the features of claim 1 that are not taught or suggest by Blandy as noted above. Accordingly, Applicants respectfully submit that claims 6, 8, and 9 patentably distinguish over the cited references for at least the reasons given above for claim 1.

In addition, claim 8 recites "wherein at least a portion of the first instruction comprises an encoding equivalent to a test NaT instruction that specifies a NaT0 from an Itanium® family instruction set architecture." Neither Blandy nor Johnson teach or suggest this feature of claim 8. Accordingly, Applicants respectfully submit that claim 8 patentably distinguishes over the cited references for at least this additional reason.

Applicants respectfully submit that Christie does not teach or suggest the features of claim 10 that are not taught or suggest by Blandy as noted above. Accordingly, Applicants respectfully submit that claims 15 and 17 patentably distinguish over the cited references for at least the reasons given above for claim 10.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-12, 15-18, 20, 23, and 25-32 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-12, 15-18, 20, 23, and 25-32 is respectfully requested.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Christopher P. Kosh at Telephone No. (512) 241-2403, Facsimile No. (512) 241-2409, or David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 22nd day of June, 2006.

By
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